



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Am

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,787	08/08/2001	Sung-Bae Park	SAM-0234	2796
7590	11/19/2003		EXAMINER	
Steven M. Mills MILLS & ONELLO LLP Suite 605 Eleven Beacon Street Boston, MA 02108			LEWIS, MONICA	
			ART UNIT	PAPER NUMBER
			2822	
DATE MAILED: 11/19/2003				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/924,787	PARK ET AL.
	Examiner Monica Lewis	Art Unit 2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 22 September 2003.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) 7 and 8 is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-6 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 08 August 2001 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____.
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>12</u> .	6) <input type="checkbox"/> Other: _____.

DETAILED ACTION

1. This office action is in response to the request for continued examination filed September 22, 2003.

Response to Arguments

2. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 3 and 4 are rejected under 35 U.S.C. 103(a) as obvious over Applicant's Prior Art Drawings in view of Christensen et al. (U.S. Patent No. 6,121,659), Hsu et al. (U.S. Patent No. 5,804,858) and Noble (U.S. Patent No. 6,156,589).

In regards to claim 1, Applicant's Prior Art Drawings disclose the following:

- a) a semiconductor substrate (20) (For Example: See Figure 2);
- b) a buried oxide layer (21) formed on the semiconductor substrate (For Example: See Figure 2);
- c) a body (14, 15) on the buried oxide layer, the body being an active region of a transistor (For Example: See Figure 2);
- d) a gate oxide layer (18) formed on a body (For Example: See Figure 2);
- e) a gate (16) formed on the gate oxide layer (For Example: See Figure 2);

f) an isolation region (11) adjacent to and at least partially surrounding the body
(For Example: See Figure 2); and

g) a body contact (12) supplying power to the body (For Example: See Figure 2).

In regards to claim 1, Applicant's Prior Art Drawings fail to disclose the following:

a) a trench that perforates the isolation region, the body, and the buried oxide layer and filling the trench with a conductive material so that the body is electrically connected to the semiconductor substrate.

However, Christensen et al. ("Christensen") discloses a trench filled with conductive material that perforates various layers (For Example: See Figure 5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include a trench, which is filled with conductive material, that perforates various layers as disclosed in Christensen because it aids in providing an electrical interconnection among the devices (For Example: See Column 5 Lines 64 and 65).

Additionally, since Applicant's Prior Art Drawings and Christensen are both from the same field of endeavor, the purpose disclosed by Christensen would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

b) a field oxide region formed in the isolation region, the field oxide region at least partially surrounding the body contact.

However, Hsu et al. ("Hsu") discloses field oxide at least partially surrounding a body contact (For Example: See Figure 5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include field oxide at least partially surrounding a body contact as

Art Unit: 2822

disclosed in Hsu because it aids in preventing a sacrifice in drain current (For Example: See Column 4 Lines 28-35).

Additionally, since Applicant's Prior Art Drawings and Hsu are both from the same field of endeavor, the purpose disclosed by Hsu would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

c) the conductive material including a silicon epitaxial layer.

However, Noble discloses the use of a silicon epitaxial layer (For Example: See Column 6 Lines 13-18). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include silicon epitaxial layer as disclosed in Noble because it aids in providing a connection among various components (For Example: See Column 6 Lines 213-18).

Additionally, since Applicant's Prior Art Drawings and Noble are both from the same field of endeavor, the purpose disclosed by Noble would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

In regards to claim 3, Applicant's Prior Art Drawings fail to disclose the following:

a) the conductive material formed of one material selected from the group consisting of a metal layer, a tungsten layer, a silicon epitaxial layer, and a combination layer of at least two of a metal layer, a tungsten layer and a silicon epitaxial layer.

However, Noble discloses the use of a silicon epitaxial layer (For Example: See Column 6 Lines 13-18). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include silicon epitaxial layer as disclosed in Noble because it aids in providing a connection among various components (For Example: See Column 6 Lines 213-18).

Additionally, since Applicant's Prior Art Drawings and Noble are both from the same field of endeavor, the purpose disclosed by Noble would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

In regards to claim 4, Applicant's Prior Art Drawings disclose the following:

a) a region into which predetermined impurity ions are implanted and generated on the semiconductor substrate in contact with the lower portion of the body contact so that an ohmic contact (110) is formed between the body contact and the semiconductor substrate (For Example: See Figure 3).

5. Claim 2 is rejected under 35 U.S.C. 103(a) as obvious over Applicant's Prior Art Drawings in view of Christensen et al. (U.S. Patent No. 6,121,659), Hsu et al. (U.S. Patent No. 5,804,858), Noble (U.S. Patent No. 6,156,589) and Wolf *Silicon Processing for the VLSI Era*.

In regards to claim 2, Applicant's Prior Art Drawings fail to disclose the following:

a) gate is formed of at least one material selected from the group consisting of metal and polysilicon.

However, Wolf discloses a gate that is composed of metal or polysilicon (For Example: See Page 318 5.3.2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include a gate composed of a metal or polysilicon as disclosed in Wolf because it aids in reducing parasitic overlap capacitances (For Example: See Page 318 5.3.2).

Additionally, since Applicant's Prior Art Drawings and Wolf are both from the same field of endeavor, the purpose disclosed by Wolf would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

Art Unit: 2822

6. Claim 5 is rejected under 35 U.S.C. 103(a) as obvious over Applicant's Prior Art Drawings in view of Christensen et al. (U.S. Patent No. 6,121,659), Hsu et al. (U.S. Patent No. 5,804,858), Noble (U.S. Patent No. 6,156,589) and Lynch et al. (U.S. Patent No. 4,646,123).

In regards to claim 5, Applicant's Prior Art Drawings fail to disclose the following:

- a) the trench narrows as the trench deepens.

However, Lynch et al. ("Lynch") discloses a trench that narrows as it deepens (For Example: See Figure 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include a trench that narrows as it deepens as disclosed in Lynch because it aids in keeping voids from forming (For Example: See Column 3 Lines 4-27).

Additionally, since Applicant's Prior Art Drawings and Lynch are both from the same field of endeavor, the purpose disclosed by Lynch would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as obvious over Applicant's Prior Art Drawings in view of Christensen et al. (U.S. Patent No. 6,121,659), Hsu et al. (U.S. Patent No. 5,804,858), Noble (U.S. Patent No. 6,156,589), Lynch et al. (U.S. Patent No. 4,646,123) and Brown et al. (U.S. Patent No. 6,476,445).

In regards to claim 6, Applicant's Prior Art Drawings fail to disclose the following:

- a) the trench narrows in a stepwise manner as the trench deepens.

However, Brown et al. ("Brown") discloses a trench that narrows in a stepwise manner (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art

Art Unit: 2822

Drawings to include a trench that narrows in a step wise manner as disclosed in Brown because it aids in permitting a variety of devices to coexist on the same substrate (For Example: See Column 4 Lines 20-41).

Additionally, since Applicant's Prior Art Drawings and Brown are both from the same field of endeavor, the purpose disclosed by Brown would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
November 14, 2003



AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800